# APPENDIX A: JOINT CLAIM CONSTRUCTION CHART

Pursuant to P.R.4-5(d), Plaintiff TQ Delta, LLC and Defendants CommScope Holding Company, Inc., CommScope Inc., ARRIS US Holdings, Inc., ARRIS Solutions, Inc., ARRIS Technology, Inc., and ARRIS Enterprises, LLC (the "CommScope Defendants") and Defendants Nokia of America Corp., Nokia Corp. and Nokia Solutions and Networks Oy (the "Nokia Defendants") hereby provide an Amended Joint Claim Construction Chart containing the disputed claim terms and phrases for the disputed claims for US Patent No. 7,570,686 ("the '686 Patent"); US Patent No. 7,453,881 ("the '881 Patent"); US Patent No. 8,276,048 ("the '048 Patent"); US Patent No. 7,844,882 ("the '882 Patent"); US Patent No. 8,090,008 ("the '008 Patent"); US Patent No. 8,462,835 ("the '835 Patent"); US Patent No. 10,567,112 ("the '112 Patent"); US Patent No. 8,468,411 ("the '411 Patent"); US Patent No. 9,094,348 ("the '348 Patent"); US Patent No. 10,833,809 ("the '809 Patent"); US Patent No. 9,485,055 ("the '055 Patent"); US Patent No. 9,154,354 ("the '354 Patent"); US Patent No. 8,937,988 ("the '988 Patent"); US Patent No. 9,014,193 ("the '193 Patent"); US Patent No. 9,300,601 ("the '601 Patent"); US Patent No. 9,894,014 ("the '014 Patent"); US Patent No. 8,495,473 ("the '5473 Patent"); US Patent No. 9,547,608 ("the '608 Patent"); US Patent No. 10,409,510 ("the '510 Patent"); US Patent No. 8,594,162 ("the '162 Patent"); US Patent No. 8,595,577 ("the '577 Patent"); US Patent No. 10,044,473 ("the '4473 Patent"). The second column refers to the term numbers in the Joint Claim Construction Chart and Prehearing Statement (Dkt. 107, Exhibits A-B); TQ Delta, LLC's Preliminary Election of Asserted Claims and the term numbers that the parties used in their claim construction briefs. In addition, the parties hereby identify the claim number(s) where the disputed terms and phrases appear.

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| "transceiver"<br><br>Family 1<br>'686 Patent, claims 17, 36, and 37<br><br>'686 Patent<br>17. An information storage media comprising instructions that when executed communicate diagnostic information over a communication channel using multicarrier modulation comprising: instructions that when executed direct a **transceiver** to receive or transmit an initiate diagnostic mode message; and instructions that when executed transmit a diagnostic message from the transceiver using multicarrier modulation, wherein the diagnostic message comprises a plurality of data variables representing the diagnostic information about the communication channel and each bit in the diagnostic message is mapped to at least one DMT symbol, and wherein one variable comprises an array representing frequency domain received idle channel noise information.<br><br>36. An information storage media comprising instructions that when | 1 | Plain and ordinary meaning, which is: "communications device capable of transmitting and receiving data wherein the transmitter portion and receiver portion share at least some common circuitry." | Plain and ordinary meaning, which is "communications device capable of transmitting and receiving data" | |

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| executed communicate diagnostic information over a communication channel using multicarrier modulation comprising: instructions that when executed direct a **transceiver** to receive or transmit an initiate diagnostic mode message; and instructions that when executed transmit from the **transceiver** a diagnostic message using multicarrier modulation with DMT symbols that are mapped to one bit of the diagnostic message, wherein the diagnostic message comprises a plurality of data variables representing the diagnostic information about the communication channel, and wherein one variable comprises an array representing is frequency domain received idle channel noise information.<br><br>37. The media of claim 36, wherein the initiate diagnostic mode message is based on at least one of an initialization failure, a bit rate failure, a CRC error in an initialization message, a CRC error during the normal steady state transmission mode, a forward error correction error, a user request and a CO technician request.<br><br><u>Family 2</u> | | | | |

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| '881 Patent, claims 17, 18, and 23<br>'193 Patent, claims 1 and 9<br>'601 Patent, claims 8 and 15<br>'014 Patent, claims 1 and 3<br><br><u>'881 Patent</u><br>17. A plurality of bonded **transceivers**, each bonded **transceiver** utilizing at least one transmission parameter value to reduce a difference in latency between the bonded **transceivers**, wherein a data rate for a first of the bonded **transceivers** is different than a data rate for a second of the bonded **transceivers**.<br><br>18. The **transceivers** of claim 17, wherein the at least one transmission parameter value is a Reed Solomon Coding parameter value, an interleaving parameter value, a coding parameter value, a codeword size value or a framing parameter value.<br><br>23. The **transceivers** of claim 17, wherein the at least one transmission parameter value for the first transceiver is a first interleaving parameter value that is different than a second interleaving parameter value for the second transceiver. | | | | |

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| '193 Patent<br>1. A device comprising: a plurality of **transceivers** configurable to simultaneously operate with a combination of bonded and unbonded transceivers, wherein a first **transceiver** of the plurality of transceivers is operable at a first data rate, and a second **transceiver** of the plurality of **transceivers** is simultaneously operable at a second data rate that is different than the first data rate, wherein the first and second **transceivers** are operable as bonded **transceivers** and wherein a third **transceiver**, of the plurality of **transceivers**, is simultaneously operable at a third data rate and the third **transceiver** is not bonded with any other **transceiver**.<br><br>9. A device comprising: a plurality of **transceivers** configurable to simultaneously operate with a combination of bonded and unbonded **transceivers**, wherein a first **transceiver** of the plurality of **transceivers** transmits at a first data rate, and a second **transceiver** of the plurality of | | | | |

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| **transceivers** simultaneously transmits at a second data rate that is different than the first data rate, wherein the first and second **transceivers** operate as bonded **transceivers** and wherein a third **transceiver**, of the plurality of **transceivers**, simultaneously transmits at a third data rate and the third **transceiver** is not bonded with any other **transceiver**.<br><br>'601 Patent<br>8. A device comprising: a plurality of **transceivers**, wherein a first **transceiver** of the plurality of **transceivers** is operable to transmit at a first data rate on a first twisted-pair line, and a second **transceiver** of the plurality of **transceivers** is simultaneously operable to transmit at a second data rate on a second twisted-pair line, wherein the first data rate and the second data rate are capable of being different and wherein the first and second twisted-pair lines are capable of providing DSL service to a first subscriber, and wherein a third **transceiver**, of the plurality of **transceivers**, is simultaneously operable to transmit at a third data rate on a third | | | | |

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| twisted-pair line, wherein the third twisted-pair line is capable of providing DSL service to a second subscriber, wherein the first and second **transceivers** are connected to a multi-pair multiplexer.<br><br>15. A device comprising: a multi-pair multiplexer, and a plurality of **transceivers**, including: a first **transceiver**, a second **transceiver**, and a third **transceiver**, the device capable of bonding at least the first and second **transceivers** of the plurality of **transceivers**, while at least the third **transceiver** of the plurality of **transceivers** is not bonded with any other **transceivers** in the device, and wherein the at least two bonded **transceivers** are operable at different data rates, and wherein the first and second **transceivers** are connected to multi-pair multiplexer and the third **transceiver** is not connected to the multi-pair multiplexer.<br><br><u>'014 Patent</u><br>1. A device comprising: plurality of **transceivers** configurable to | | | | |

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| simultaneously operate with a combination of bonded and unbonded **transceivers**, wherein a first **transceiver** of the plurality of **transceivers** is operable at a first data rate, and a second **transceiver** of the plurality of **transceivers** is simultaneously operable at a second data rate that is different than the first data rate, wherein the first and second **transceivers** are operable as bonded **transceivers**, and wherein a third **transceiver**, of the plurality of **transceivers**, is simultaneously operable at a third data rate, different than the first data rate and the second data rate, and the third **transceiver** is not bonded with any other **transceiver**, wherein the first and second **transceivers** are VDSL transceivers that are operable to transmit Internet Protocol (IP) packets, and wherein the third **transceiver** is a ADSL **transceiver** operable to transmit ATM cells.<br><br>3. The device of claim 1, wherein the first and second **transceivers** generate a single high data rate connection between a service provider and a subscriber.<br><br><u>Family 3</u> | | | | |

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| '882 Patent, claims 9 and 13<br>'048 Patent, claims 1 and 5<br>'5473 Patent, claims 10 and 28<br>'608 Patent, claim 2<br>'510 Patent, claim 22<br><br>'882 Patent<br>9. A system that allocates shared memory comprising: a **transceiver** that performs: transmitting or receiving a message during initialization specifying a maximum number of bytes of memory that are available to be allocated to an interleaver; determining an amount of memory required by the interleaver to interleave a first plurality of Reed Solomon (RS) coded data bytes within a shared memory; allocating a first number of bytes of the shared memory to the interleaver to interleave the first plurality of Reed Solomon (RS) coded data bytes for transmission at a first data rate, wherein the allocated memory for the interleaver does not exceed the maximum number of bytes specified in the message; allocating a second number of bytes of the shared memory to a deinterleaver to deinterleave a second plurality of RS coded data bytes received | | | | |

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| at a second data rate; and interleaving the first plurality of RS coded data bytes within the shared memory allocated to the interleaver and deinterleaving the second plurality of RS coded data bytes within the shared memory allocated to the deinterleaver, wherein the shared memory allocated to the interleaver is used at the same time as the shared memory allocated to the deinterleaver.<br><br>13. A system that allocates shared memory comprising: a **transceiver** that performs: transmitting or receiving a message during initialization specifying a maximum number of bytes of memory that are available to be allocated to a deinterleaver; determining an amount of memory required by the deinterleaver to deinterleave a first plurality of Reed Solomon (RS) coded data bytes within a shared memory; allocating a first number of bytes of the shared memory to the deinterleaver to deinterleave a first plurality of Reed Solomon (RS) coded data bytes for transmission at a first data rate, wherein the allocated memory for the deinterleaver does not exceed the maximum number of bytes specified in the message; allocating a second number | | | | |

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| of bytes of the shared memory to an interleaver to interleave a second plurality of RS coded data bytes received at a second data rate; and deinterleaving the first plurality of RS coded data bytes within the shared memory allocated to the deinterleaver and interleaving the second plurality of RS coded data bytes within the shared memory allocated to the interleaver, wherein the shared memory allocated to the deinterleaver is used at the same time as the shared memory allocated to the interleaver.<br><br>'048 Patent<br>1. A system that allocates shared memory comprising: a **transceiver** that is capable of: transmitting or receiving a message during initialization specifying a maximum number of bytes of memory that are available to be allocated to an interleaver; determining an amount of memory required by the interleaver to interleave a first plurality of Reed Solomon (RS) coded data bytes within the shared memory; allocating a first number of bytes of the shared memory to the interleaver to interleave the first plurality of Reed Solomon (RS) coded | | | | |

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| data bytes for transmission at a first data rate, wherein the allocated memory for the interleaver does not exceed the maximum number of bytes specified in the message; allocating a second number of bytes of the shared memory to a deinterleaver to deinterleave a second plurality of RS coded data bytes received at a second data rate; and interleaving the first plurality of RS coded data bytes within the shared memory allocated to the interleaver and deinterleaving the second plurality of RS coded data bytes within the shared memory allocated to the deinterleaver, wherein the shared memory allocated to the interleaver is used at the same time as the shared memory allocated to the deinterleaver.<br><br>5. A system that allocates shared memory comprising: a **transceiver** that is capable of: transmitting or receiving a message during initialization specifying a maximum number of bytes of memory that are available to be allocated to a deinterleaver; determining an amount of memory required by the deinterleaver to deinterleave a first plurality of Reed Solomon (RS) coded data bytes within the shared memory; allocating a first | | | | |

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| number of bytes of the shared memory to the deinterleaver to deinterleave a first plurality of Reed Solomon (RS) coded data bytes for transmission at a first data rate, wherein the allocated memory for the deinterleaver does not exceed the maximum number of bytes specified in the message; allocating a second number of bytes of the shared memory to an interleaver to interleave a second plurality of RS coded data bytes received at a second data rate; and deinterleaving the first plurality of RS coded data bytes within the shared memory allocated to the deinterleaver and interleaving the second plurality of RS coded data bytes within the shared memory allocated to the interleaver, wherein the shared memory allocated to the deinterleaver is used at the same time as the shared memory allocated to the interleaver.<br><br>'5473 Patent<br>10. A multicarrier communications **transceiver** with a shared memory, the **transceiver** capable of: sharing the memory between an interleaver in a first latency path and a deinterleaver in a second latency path; and transmitting or | | | | |

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| receiving, during initialization of the transceiver, a message indicating how the shared memory is to be used by the interleaver or the deinterleaver.<br><br>28. An apparatus comprising: a multicarrier communications **transceiver** that is configured to generate a message during an initialization of the **transceiver**, perform an interleaving function associated with a first latency path, and perform a deinterleaving function associated with a second latency path, the **transceiver** being associated with a memory, wherein at least a portion of the memory may be allocated to the interleaving function or the deinterleaving function at any one particular time and wherein the generated message indicates how the memory has been allocated between the interleaving function and the deinterleaving function.<br><br><u>'608 Patent</u><br>2. The **transceiver** of claim 1, further comprising a memory wherein the memory is operable to be shared between the interleaver function of the transmitter portion associated with the transmit | | | | |

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| latency path and the deinterleaver function of the receiver portion associated with the receive latency path, wherein the first maximum number of bytes associated with the interleaver function is used to determine how much memory is used by the interleaver function and wherein the first maximum number of bytes associated with the deinterleaver function is used to determine how much memory is used by the deinterleaver function, wherein the sharing comprises using a first portion of the memory for the interleaver function and simultaneously using a second portion of the memory, different than the first portion, for the deinterleaver function, and the first and second portions of the memory are configurable such that one or more bytes of the memory can be used by the interleaver function at one particular time and the same one or more bytes of the memory can be used by the deinterleaver function at a second time, different than the first time.<br><br>'510 Patent | | | | |

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| 22. The device of claim 21, wherein the **transceiver** is further operable to transmit to another **transceiver** information that indicates the updated shared memory allocation between the interleaver and the deinterlever.<br><br><u>Family 6</u><br>'835 Patent, claim 8<br>'112 Patent, claims 8 and 10<br><br><u>'835 Patent</u><br>8. An apparatus configurable to adapt forward error correction and interleaver parameter (FIP) settings during steady-state communication or initialization comprising: a **transceiver**, including a processor, configurable to: transmit a signal using a first FIP setting, transmit a flag signal, and switch to using for transmission, a second FIP setting following transmission of the flag signal, wherein: the first FIP setting comprises at least one first FIP value, the second FIP setting comprises at least one second FIP value, different than the first FIP value, and the switching occurs on a pre-defined forward error correction | | | | |

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| codeword boundary following the flag signal.<br><br>'112 Patent<br>8. A **transceiver** comprising: a receiver operable to receiving, during steady-state communication, using a first forward error correction and interleaving parameter (FIP) setting that comprises a forward error correction (FEC) codeword size and a first number of FEC coding parity bytes; and the receiver further operable to switch, during the steady-state communication, to receiving using a second FIP setting that comprises a second FEC codeword size that is different than the first FEC codeword size and a second number of FEC coding parity bytes that is different than the first number of FEC coding parity bytes, wherein the switching to receiving using the second FEC codeword size and the second number of FEC coding parity bytes is based on a counter reaching a value.<br><br>10. The **transceiver** of claim 8, wherein the switching to receiving using the second FEC codeword size and the | | | | |

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| second number of FEC coding parity bytes does not cause bit errors or service interruption.<br><br>Family 9<br>'411 Patent, claim 10 and 18<br>'577 Patent, claim 16<br>'348 Patent, claims 1 and 9<br>'055 Patent, claims 11 and 17<br>'809 Patent, claims 4, 6, 8, 11, and 13<br><br>'411 Patent<br>10. A **transceiver** capable of packet retransmission comprising: a transmitter portion capable of: transmitting a plurality of packets, identifying at least one packet of the plurality of packets as a packet that should be retransmitted and allocating a memory between a retransmission function and an interleaving and/or deinterleaving function, wherein at least a portion of the memory may be allocated to the retransmission function or to the interleaving and/or deinterleaving function at any one particular time, and wherein a message transmitted during initialization indicates how the memory has been allocated between the | | | | |

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| retransmission function and the interleaving and/or deinterleaving function in the transceiver.<br><br>18. A **transceiver** capable of packet retransmission comprising: a receiver portion capable of: receiving a plurality of packets, identifying at least one packet of the plurality of packets as a packet that should be retransmitted and allocating a memory between a retransmission function and an interleaving and/or deinterleaving function wherein the memory is allocated between the interleaving function and the deinterleaving function in accordance with a message received during an initialization of the transceiver and wherein at least a portion of the memory may be allocated between the retransmission function and the interleaving and/or deinterleaving function at any one particular time depending on the message.<br><br>'577 Patent<br>16. An apparatus comprising: a multicarrier **transceiver** operable to receive at least one packet using deinterleaving, and transmit at least one | | | | |

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| message without using interleaving, wherein the at least one message includes information that indicates an acknowledgement (ACK) or a negative acknowledgement (NACK) of the at least one packet, wherein the at least one packet comprises one or more PTM-TC codewords.<br><br>'348 Patent<br>1. An apparatus comprising: a multicarrier **transceiver** including a processor and memory operable to: transmit a packet using a forward error correction encoder and an interleaver, wherein the packet comprises a header field and a plurality of PTM-TC codewords, a plurality of ATM cells or a plurality of Reed-Solomon codewords, and wherein the header field comprises a sequence identifier (SID); and receive a plurality of messages using a forward error correction decoder and without using a deinterleaver, wherein each message of the plurality of messages is received in a different DMT symbol and wherein at least one message of the plurality of messages includes an acknowledgement (ACK) or a negative | | | | |

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| acknowledgement (NACK) of the transmitted packet.<br><br>9. An apparatus comprising: a multicarrier **transceiver** including a processor and memory operable to: receive a packet using a forward error correction decoder and a deinterleaver, wherein the packet comprises a header field and a plurality of PTM-TC codewords, a plurality of ATM cells or a plurality of Reed-Solomon codewords, and wherein the header field comprises a sequence identifier (SID); and transmit a plurality of messages using a forward error correction encoder and without using an interleaver, wherein each message of the plurality of messages is transmitted in a different DMT symbol and wherein at least one message of the plurality of messages includes an acknowledgement (ACK) or a negative acknowledgement (NACK) of the received packet.<br><br><u>'055 Patent</u><br>11. A **transceiver** operable to transmit a first type of packet and to transmit a second type of packet, wherein the first | | | | |

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| type of packet is stored in a retransmission buffer after transmission and the second type of packet is not stored in a retransmission buffer after transmission, and wherein the first and second types of packet comprise a header field that indicates whether a transmitted packet is a first type of packet or a second type of packet, and wherein the header field of the first type of packet comprises a sequence identifier (SID) that is incremented after the first type of packet is transmitted and the header field of the second type of packet does not comprise the SID of the first type of packet.<br><br>17. The **transceiver** of claim 11, wherein the first type of packet comprises one or more PTM-TC (Packet Transfer Mode-Transmission Convergence) codewords.<br><br><u>'809 Patent</u><br>4. The apparatus of claim 1, wherein a physical layer of the **transceiver** is capable of generating the packet and the message.<br><br>6. The apparatus of claim 2, wherein a physical layer of the **transceiver** is | | | | |

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| capable of generating the packet and the message.<br><br>8. An apparatus comprising: a multicarrier **transceiver** including a processor and memory capable of: receiving a packet using forward error correction decoding and deinterleaving, wherein the packet comprises a header field and a plurality of Reed-Solomon codewords, and wherein the header field comprises a sequence identifier (SID); and transmitting a message using forward error correction encoding and without using interleaving, wherein the message is transmitted in a single DMT symbol and wherein the message includes an acknowledgement (ACK) or a negative acknowledgement (NACK) of the received packet.<br><br>11. The apparatus of claim 8, wherein a physical layer of the **transceiver** is capable of generating the packet and the message.<br><br>13. The apparatus of claim 9, wherein a physical layer of the **transceiver** is capable of generating the packet and the message. | | | | |

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| "configurable to" / "operable" / "operable to"<br><br>Family 2<br>'193 Patent, claims 1 and 9<br>'601 Patent, claim 8<br>'014 Patent, claim 1<br><br>'193 Patent<br>1. A device comprising: a plurality of transceivers **configurable to** simultaneously operate with a combination of bonded and unbonded transceivers, wherein a first transceiver of the plurality of transceivers is **operable** at a first data rate, and a second transceiver of the plurality of transceivers is simultaneously **operable** at a second data rate that is different than the first data rate, wherein the first and second transceivers are **operable** as bonded transceivers and wherein a third transceiver, of the plurality of transceivers, is simultaneously **operable** at a third data rate and the third transceiver is not bonded with any other transceiver.<br><br>9. A device comprising: a plurality of transceivers **configurable to** | 2 | Plain and ordinary meaning, which is: "able to be configured" / "capable" / "capable to" | Plain and ordinary meaning, not mere capability | |

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| simultaneously operate with a combination of bonded and unbonded transceivers, wherein a first transceiver of the plurality of transceivers transmits at a first data rate, and a second transceiver of the plurality of transceivers simultaneously transmits at a second data rate that is different than the first data rate, wherein the first and second transceivers operate as bonded transceivers and wherein a third transceiver, of the plurality of transceivers, simultaneously transmits at a third data rate and the third transceiver is not bonded with any other transceiver.<br><br><u>'601 Patent</u><br>8. A device comprising: a plurality of transceivers, wherein a first transceiver of the plurality of transceivers is **operable to** transmit at a first data rate on a first twisted-pair line, and a second transceiver of the plurality of transceivers is simultaneously **operable to** transmit at a second data rate on a second twisted-pair line, wherein the first data rate and the second data rate are capable of being different and wherein the first and second twisted-pair lines are | | | | |

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| capable of providing DSL service to a first subscriber, and wherein a third transceiver, of the plurality of transceivers, is simultaneously **operable to** transmit at a third data rate on a third twisted-pair line, wherein the third twisted-pair line is capable of providing DSL service to a second subscriber, wherein the first and second transceivers are connected to a multi-pair multiplexer.<br><br>'014 Patent<br>1. A device comprising: plurality of transceivers **configurable to** simultaneously operate with a combination of bonded and unbonded transceivers, wherein a first transceiver of the plurality of transceivers is **operable** at a first data rate, and a second transceiver of the plurality of transceivers is simultaneously **operable** at a second data rate that is different than the first data rate, wherein the first and second transceivers are **operable** as bonded transceivers, and wherein a third transceiver, of the plurality of transceivers, is simultaneously **operable** at a third data rate, different than the first data rate and the second data rate, and | | | | |

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| the third transceiver is not bonded with any other transceiver, wherein the first and second transceivers are VDSL transceivers that are **operable** to transmit Internet Protocol (IP) packets, and wherein the third transceiver is a ADSL transceiver **operable** to transmit ATM cells.<br><br><u>Family 3</u><br>'608 Patent, claim 2<br>'510 Patent, claim 22<br><br><u>'608 Patent</u><br>2. The transceiver of claim 1, further comprising a memory wherein the memory is **operable to** be shared between the interleaver function of the transmitter portion associated with the transmit latency path and the deinterleaver function of the receiver portion associated with the receive latency path, wherein the first maximum number of bytes associated with the interleaver function is used to determine how much memory is used by the interleaver function and wherein the first maximum number of bytes associated with the deinterleaver function is used to | | | | |

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| determine how much memory is used by the deinterleaver function, wherein the sharing comprises using a first portion of the memory for the interleaver function and simultaneously using a second portion of the memory, different than the first portion, for the deinterleaver function, and the first and second portions of the memory are configurable such that one or more bytes of the memory can be used by the interleaver function at one particular time and the same one or more bytes of the memory can be used by the deinterleaver function at a second time, different than the first time.<br><br><u>'510 Patent</u><br>22. The device of claim 21, wherein the transceiver is further **operable to** transmit to another transceiver information that indicates the updated shared memory allocation between the interleaver and the deinterlever.<br><br><u>Family 6</u><br>'112 Patent, claim 8 | | | | |

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| '112 Patent<br>8. A transceiver comprising: a receiver **operable to** receiving, during steady-state communication, using a first forward error correction and interleaving parameter (FIP) setting that comprises a forward error correction (FEC) codeword size and a first number of FEC coding parity bytes; and the receiver further **operable to** switch, during the steady-state communication, to receiving using a second FIP setting that comprises a second FEC codeword size that is different than the first FEC codeword size and a second number of FEC coding parity bytes that is different than the first number of FEC coding parity bytes, wherein the switching to receiving using the second FEC codeword size and the second number of FEC coding parity bytes is based on a counter reaching a value.<br><br>Family 9<br>'577 Patent, claim 16<br>'348 Patent, claims 1 and 9<br>'055 Patent, claim 11<br><br>'577 Patent | | | | |

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| 16. An apparatus comprising: a multicarrier transceiver **operable to** receive at least one packet using deinterleaving, and transmit at least one message without using interleaving, wherein the at least one message includes information that indicates an acknowledgement (ACK) or a negative acknowledgement (NACK) of the at least one packet, wherein the at least one packet comprises one or more PTM-TC codewords.<br><br>'348 Patent<br>1. An apparatus comprising: a multicarrier transceiver including a processor and memory **operable to**: transmit a packet using a forward error correction encoder and an interleaver, wherein the packet comprises a header field and a plurality of PTM-TC codewords, a plurality of ATM cells or a plurality of Reed-Solomon codewords, and wherein the header field comprises a sequence identifier (SID); and receive a plurality of messages using a forward error correction decoder and without using a deinterleaver, wherein each message of the plurality of messages is | | | | |

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| received in a different DMT symbol and wherein at least one message of the plurality of messages includes an acknowledgement (ACK) or a negative acknowledgement (NACK) of the transmitted packet.<br><br>9. An apparatus comprising: a multicarrier transceiver including a processor and memory **operable to**: receive a packet using a forward error correction decoder and a deinterleaver, wherein the packet comprises a header field and a plurality of PTM-TC codewords, a plurality of ATM cells or a plurality of Reed-Solomon codewords, and wherein the header field comprises a sequence identifier (SID); and transmit a plurality of messages using a forward error correction encoder and without using an interleaver, wherein each message of the plurality of messages is transmitted in a different DMT symbol and wherein at least one message of the plurality of messages includes an acknowledgement (ACK) or a negative acknowledgement (NACK) of the received packet. | | | | |

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| '055 Patent<br>11. A transceiver **operable to** transmit a first type of packet and to transmit a second type of packet, wherein the first type of packet is stored in a retransmission buffer after transmission and the second type of packet is not stored in a retransmission buffer after transmission, and wherein the first and second types of packet comprise a header field that indicates whether a transmitted packet is a first type of packet or a second type of packet, and wherein the header field of the first type of packet comprises a sequence identifier (SID) that is incremented after the first type of packet is transmitted and the header field of the second type of packet does not comprise the SID of the first type of packet.<br><br>Family 10<br><br>'354 Patent, claim 10<br>'988 Patent, claim 16<br><br>'354 Patent<br>10. A multicarrier communications transceiver **operable to**: receive a | | | | |

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| multicarrier symbol comprising a first plurality of carriers and a second plurality of carriers; receive a first plurality of bits on the first plurality of carriers using a first SNR margin; receive a second plurality of bits on the second plurality of carriers using a second SNR margin; wherein the first plurality of carriers is different than the second plurality of carriers, wherein the first SNR margin is different than the second SNR margin, and wherein the first SNR margin provides more robust.<br><br>'988 Patent<br>16. An apparatus comprising: a multicarrier communications transceiver **operable to** demodulate for reception a first plurality of bits from a first carrier using a first Signal to Noise Ratio (SNR) margin and to demodulate for reception a second plurality of bits from a second carrier using a second SNR margin, and to demodulate for reception a third plurality of bits from the first carrier using a third SNR margin, wherein the first SNR margin specifies a first value for an allowable increase in noise without an increase in the bit error rate | | | | |

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| (BER) associated with the first carrier, wherein the second SNR margin specifies a second value for an allowable increase in noise without an increase in the bit error rate (BER) associated with the second carrier, wherein the third SNR margin specifies a third value for an allowable increase in noise without an increase in the bit error rate (BER) associated with said first carrier, wherein the first SNR margin is different than the second SNR margin, wherein the first SNR margin is different than the third SNR margin, and wherein the first plurality of bits, the second plurality of bits and the third plurality of bits are each different from one another. | | | | |
| "each bit in the diagnostic message is mapped to at least one DMT symbol"<br><br><u>Family 1</u><br>'686 Patent, claim 17<br><br>"DMT symbols that are mapped to one bit of the diagnostic message"<br><br><u>Family 1</u><br>'686 Patent, claim 36<br><br><u>'686 Patent</u> | 3 | "each bit in the diagnostic message is communicated using a modulation scheme where a DMT symbol (or two or more DMT symbols) represents only a single bit of the diagnostic message" | Indefinite. | |

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| 17. An information storage media comprising instructions that when executed communicate diagnostic information over a communication channel using multicarrier modulation comprising: instructions that when executed direct a transceiver to receive or transmit an initiate diagnostic mode message; and instructions that when executed transmit a diagnostic message from the transceiver using multicarrier modulation, wherein the diagnostic message comprises a plurality of data variables representing the diagnostic information about the communication channel and **each bit in the diagnostic message is mapped to at least one DMT symbol**, and wherein one variable comprises an array representing frequency domain received idle channel noise information.<br><br>36. An information storage media comprising instructions that when executed communicate diagnostic information over a communication channel using multicarrier modulation comprising: instructions that when executed direct a transceiver to receive or transmit an initiate diagnostic mode | | | | |

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| message; and instructions that when executed transmit from the transceiver a diagnostic message using multicarrier modulation with **DMT symbols that are mapped to one bit of the diagnostic message**, wherein the diagnostic message comprises a plurality of data variables representing the diagnostic information about the communication channel, and wherein one variable comprises an array representing is frequency domain received idle channel noise information. | | | | |
| "array representing frequency domain received idle channel noise information"<br><br>Family 1<br>'686 Patent, claims 17 and 36<br><br>'686 Patent<br>17. An information storage media comprising instructions that when executed communicate diagnostic information over a communication channel using multicarrier modulation comprising: instructions that when executed direct a transceiver to receive or transmit an initiate diagnostic mode message; and instructions that when executed transmit a diagnostic message | 4 | "ordered set of values representative of noise in the frequency domain that was received by a transceiver on respective subchannels in the absence of a transmission signal on the received channel" | "array of values representative of noise in the frequency domain that was received by a transceiver on respective subchannels in the absence of a transmission signal" | |

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| from the transceiver using multicarrier modulation, wherein the diagnostic message comprises a plurality of data variables representing the diagnostic information about the communication channel and each bit in the diagnostic message is mapped to at least one DMT symbol, and wherein one variable comprises an **array representing frequency domain received idle channel noise information**.<br><br>36. An information storage media comprising instructions that when executed communicate diagnostic information over a communication channel using multicarrier modulation comprising: instructions that when executed direct a transceiver to receive or transmit an initiate diagnostic mode message; and instructions that when executed transmit from the transceiver a diagnostic message using multicarrier modulation with DMT symbols that are mapped to one bit of the diagnostic message, wherein the diagnostic message comprises a plurality of data variables representing the diagnostic information about the communication channel, and wherein one variable comprises an **array** | | | | |

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| **representing is frequency domain received idle channel noise information**. | | | | |
| "plurality of bonded transceivers"<br><br>Family 2<br>'881 Patent, claim 17<br><br>'881 Patent<br>17. A **plurality of bonded transceivers**, each bonded transceiver utilizing at least one transmission parameter value to reduce a difference in latency between the bonded transceivers, wherein a data rate for a first of the bonded transceivers is different than a data rate for a second of the bonded transceivers. | 5 | "two or more transceivers located on the same side of two or more physical links where each transceiver is configurable to transmit or receive a different portion of the same bit stream via a different one of the physical links" | "two or more transceivers, located on the same side of two or more physical links and each corresponding to one of the physical links, coordinated to transmit or receive a different portion of the same bit stream via a different one of the physical links" | |
| "reduce a difference in latency between the bonded transceivers"<br><br>Family 2<br>'881 Patent, claim 17<br><br>'881 Patent<br>17. A plurality of bonded transceivers, each bonded transceiver utilizing at least one transmission parameter value to **reduce a difference in latency between the bonded transceivers**, wherein a data | 6 | "reduce a difference in configuration latency" | Indefinite, or, if not indefinite, "minimize the difference in the configuration latencies between the bonded transceivers" | |

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| rate for a first of the bonded transceivers is different than a data rate for a second of the bonded transceivers. | | | | |
| "each bonded transceiver utilizing at least one transmission parameter value to reduce a difference in latency between the bonded transceivers"<br><br>Family 2<br>'881 Patent, claim 17<br><br>'881 Patent<br>17. A plurality of bonded transceivers, **each bonded transceiver utilizing at least one transmission parameter value to reduce a difference in latency between the bonded transceivers**, wherein a data rate for a first of the bonded transceivers is different than a data rate for a second of the bonded transceivers. | 7 | "reduce a difference in configuration latency" | Indefinite, or, if not indefinite, "minimize the difference in the configuration latencies between the bonded transceivers" | |
| "shared memory" / "sharing the memory" / "operable to be shared" / "sharing"<br><br>Family 3<br>'882 Patent, claims 9 and 13 ("shared memory") | 8 | "common memory used by at least two functions, where a portion of the memory can be used by either one of the functions" | Plain and ordinary meaning | |

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| '048 Patent, claims 1 and 5 ("shared memory")<br><br>'5473 Patent, claim 10 ("sharing the memory")<br><br>'608 Patent, claim 2 ("operable to be shared / sharing")<br><br>'510 Patent, claim 22 ("shared memory")<br><br><u>'882 Patent</u><br>9. A system that allocates **shared memory** comprising: a transceiver that performs: transmitting or receiving a message during initialization specifying a maximum number of bytes of memory that are available to be allocated to an interleaver; determining an amount of memory required by the interleaver to interleave a first plurality of Reed Solomon (RS) coded data bytes within a **shared memory**; allocating a first number of bytes of the **shared memory** to the interleaver to interleave the first plurality of Reed Solomon (RS) coded data bytes for transmission at a first data rate, wherein the allocated memory for the interleaver does not exceed the maximum number of bytes specified in | | | | |

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| the message; allocating a second number of bytes of the **shared memory** to a deinterleaver to deinterleave a second plurality of RS coded data bytes received at a second data rate; and interleaving the first plurality of RS coded data bytes within the **shared memory** allocated to the interleaver and deinterleaving the second plurality of RS coded data bytes within the **shared memory** allocated to the deinterleaver, wherein the **shared memory** allocated to the interleaver is used at the same time as the **shared memory** allocated to the deinterleaver.<br><br>13. A system that allocates **shared memory** comprising: a transceiver that performs: transmitting or receiving a message during initialization specifying a maximum number of bytes of memory that are available to be allocated to a deinterleaver; determining an amount of memory required by the deinterleaver to deinterleave a first plurality of Reed Solomon (RS) coded data bytes within a **shared memory**; allocating a first number of bytes of the **shared memory** to the deinterleaver to deinterleave a first plurality of Reed Solomon (RS) coded data bytes for transmission at a first data | | | | |

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| rate, wherein the allocated memory for the deinterleaver does not exceed the maximum number of bytes specified in the message; allocating a second number of bytes of the **shared memory** to an interleaver to interleave a second plurality of RS coded data bytes received at a second data rate; and deinterleaving the first plurality of RS coded data bytes within the **shared memory** allocated to the deinterleaver and interleaving the second plurality of RS coded data bytes within the **shared memory** allocated to the interleaver, wherein the **shared memory** allocated to the deinterleaver is used at the same time as the **shared memory** allocated to the interleaver.<br><br><u>'048 Patent</u><br>1. A system that allocates **shared memory** comprising: a transceiver that is capable of: transmitting or receiving a message during initialization specifying a maximum number of bytes of memory that are available to be allocated to an interleaver; determining an amount of memory required by the interleaver to interleave a first plurality of Reed Solomon (RS) coded data bytes within | | | | |

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| the **shared memory**; allocating a first number of bytes of the **shared memory** to the interleaver to interleave the first plurality of Reed Solomon (RS) coded data bytes for transmission at a first data rate, wherein the allocated memory for the interleaver does not exceed the maximum number of bytes specified in the message; allocating a second number of bytes of the **shared memory** to a deinterleaver to deinterleave a second plurality of RS coded data bytes received at a second data rate; and interleaving the first plurality of RS coded data bytes within the **shared memory** allocated to the interleaver and deinterleaving the second plurality of RS coded data bytes within the **shared memory** allocated to the deinterleaver, wherein the **shared memory** allocated to the interleaver is used at the same time as the **shared memory** allocated to the deinterleaver.<br><br>5. A system that allocates **shared memory** comprising: a transceiver that is capable of: transmitting or receiving a message during initialization specifying a maximum number of bytes of memory that are available to be allocated to a deinterleaver; determining an amount of | | | | |

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| memory required by the deinterleaver to deinterleave a first plurality of Reed Solomon (RS) coded data bytes within the **shared memory**; allocating a first number of bytes of the **shared memory** to the deinterleaver to deinterleave a first plurality of Reed Solomon (RS) coded data bytes for transmission at a first data rate, wherein the allocated memory for the deinterleaver does not exceed the maximum number of bytes specified in the message; allocating a second number of bytes of the **shared memory** to an interleaver to interleave a second plurality of RS coded data bytes received at a second data rate; and deinterleaving the first plurality of RS coded data bytes within the **shared memory** allocated to the deinterleaver and interleaving the second plurality of RS coded data bytes within the **shared memory** allocated to the interleaver, wherein the **shared memory** allocated to the deinterleaver is used at the same time as the **shared memory** allocated to the interleaver.<br><br><u>'5473 Patent</u><br>10. A multicarrier communications transceiver with a **shared memory**, the | | | | |

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| transceiver capable of: **sharing the memory** between an interleaver in a first latency path and a deinterleaver in a second latency path; and transmitting or receiving, during initialization of the transceiver, a message indicating how the **shared memory** is to be used by the interleaver or the deinterleaver.<br><br>'608 Patent<br>2. The transceiver of claim 1, further comprising a memory wherein the memory is **operable to be shared** between the interleaver function of the transmitter portion associated with the transmit latency path and the deinterleaver function of the receiver portion associated with the receive latency path, wherein the first maximum number of bytes associated with the interleaver function is used to determine how much memory is used by the interleaver function and wherein the first maximum number of bytes associated with the deinterleaver function is used to determine how much memory is used by the deinterleaver function, wherein the **sharing** comprises using a first portion of the memory for the interleaver | | | | |

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| function and simultaneously using a second portion of the memory, different than the first portion, for the deinterleaver function, and the first and second portions of the memory are configurable such that one or more bytes of the memory can be used by the interleaver function at one particular time and the same one or more bytes of the memory can be used by the deinterleaver function at a second time, different than the first time.<br><br><u>'510 Patent</u><br>22. The device of claim 21, wherein the transceiver is further operable to transmit to another transceiver information that indicates the updated **shared memory** allocation between the interleaver and the deinterlever. | | | | |
| "wherein the generated message indicates how the memory has been allocated between the [first deinterleaving / interleaving] function and the [second] deinterleaving function" / "a message indicating how the shared memory is to be used by the interleaver or the deinterleaver" | 9 | Plain and ordinary meaning. No construction necessary. | Plain and ordinary meaning, i.e., "the message indicates the amount of memory [that has been allocated to / is to be used by] the [first deinterleaving / interleaving] function and | |

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| Family 3<br>'5473 Patent, claims 10 and 28<br><br>'5473 Patent<br>10. A multicarrier communications transceiver with a shared memory, the transceiver capable of: sharing the memory between an interleaver in a first latency path and a deinterleaver in a second latency path; and transmitting or receiving, during initialization of the transceiver, a **message indicating how the shared memory is to be used by the interleaver or the deinterleaver**.<br><br>28. An apparatus comprising: a multicarrier communications transceiver that is configured to generate a message during an initialization of the transceiver, perform an interleaving function associated with a first latency path, and perform a deinterleaving function associated with a second latency path, the transceiver being associated with a memory, wherein at least a portion of the memory may be allocated to the interleaving function or the deinterleaving function at any one | | | the amount of memory [that has been allocated to / is to be used by] the [second] deinterleaving function" | |

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| particular time and **wherein the generated message indicates how the memory has been allocated between the interleaving function and the deinterleaving function**. | | | | |
| "specifying a maximum number of bytes of memory that are available to be allocated to [a/an interleaver/deinterleaver]"<br><br>Family 3<br>'882 Patent, claims 9 and 13<br>'048 Patent, claim 1 and 5<br><br>'882 Patent<br>9. A system that allocates shared memory comprising: a transceiver that performs: transmitting or receiving a message during initialization **specifying a maximum number of bytes of memory that are available to be allocated to an interleaver**; determining an amount of memory required by the interleaver to interleave a first plurality of Reed Solomon (RS) coded data bytes within a shared memory; allocating a first number of bytes of the shared memory to the interleaver to interleave the first plurality of Reed Solomon (RS) coded data bytes for transmission at a first data rate, | 10 | Plain and ordinary meaning. No construction necessary. | Plain and ordinary meaning. | |

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| wherein the allocated memory for the interleaver does not exceed the maximum number of bytes specified in the message; allocating a second number of bytes of the shared memory to a deinterleaver to deinterleave a second plurality of RS coded data bytes received at a second data rate; and interleaving the first plurality of RS coded data bytes within the shared memory allocated to the interleaver and deinterleaving the second plurality of RS coded data bytes within the shared memory allocated to the deinterleaver, wherein the shared memory allocated to the interleaver is used at the same time as the shared memory allocated to the deinterleaver.<br><br>13. A system that allocates shared memory comprising: a transceiver that performs: transmitting or receiving a message during initialization **specifying a maximum number of bytes of memory that are available to be allocated to a deinterleaver**; determining an amount of memory required by the deinterleaver to deinterleave a first plurality of Reed Solomon (RS) coded data bytes within a shared memory; allocating a first number of bytes of the shared memory to the | | | | |

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| deinterleaver to deinterleave a first plurality of Reed Solomon (RS) coded data bytes for transmission at a first data rate, wherein the allocated memory for the deinterleaver does not exceed the maximum number of bytes specified in the message; allocating a second number of bytes of the shared memory to an interleaver to interleave a second plurality of RS coded data bytes received at a second data rate; and deinterleaving the first plurality of RS coded data bytes within the shared memory allocated to the deinterleaver and interleaving the second plurality of RS coded data bytes within the shared memory allocated to the interleaver, wherein the shared memory allocated to the deinterleaver is used at the same time as the shared memory allocated to the interleaver.<br><br>'048 Patent<br>1. A system that allocates shared memory comprising: a transceiver that is capable of: transmitting or receiving a message during initialization **specifying a maximum number of bytes of memory that are available to be allocated to an interleaver**; determining an amount of | | | | |

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| memory required by the interleaver to interleave a first plurality of Reed Solomon (RS) coded data bytes within the shared memory; allocating a first number of bytes of the shared memory to the interleaver to interleave the first plurality of Reed Solomon (RS) coded data bytes for transmission at a first data rate, wherein the allocated memory for the interleaver does not exceed the maximum number of bytes specified in the message; allocating a second number of bytes of the shared memory to a deinterleaver to deinterleave a second plurality of RS coded data bytes received at a second data rate; and interleaving the first plurality of RS coded data bytes within the shared memory allocated to the interleaver and deinterleaving the second plurality of RS coded data bytes within the shared memory allocated to the deinterleaver, wherein the shared memory allocated to the interleaver is used at the same time as the shared memory allocated to the deinterleaver.<br><br>5. A system that allocates shared memory comprising: a transceiver that is capable of: transmitting or receiving a message during initialization **specifying a** | | | | |

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| **maximum number of bytes of memory that are available to be allocated to a deinterleaver**; determining an amount of memory required by the deinterleaver to deinterleave a first plurality of Reed Solomon (RS) coded data bytes within the shared memory; allocating a first number of bytes of the shared memory to the deinterleaver to deinterleave a first plurality of Reed Solomon (RS) coded data bytes for transmission at a first data rate, wherein the allocated memory for the deinterleaver does not exceed the maximum number of bytes specified in the message; allocating a second number of bytes of the shared memory to an interleaver to interleave a second plurality of RS coded data bytes received at a second data rate; and deinterleaving the first plurality of RS coded data bytes within the shared memory allocated to the deinterleaver and interleaving the second plurality of RS coded data bytes within the shared memory allocated to the interleaver, wherein the shared memory allocated to the deinterleaver is used at the same time as the shared memory allocated to the interleaver. | | | | |

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| "phase characteristic(s)" / "each carrier signal has a phase characteristic associated with the bit stream"<br><br>Family 4<br>'008 Patent, claim 14<br><br>'008 Patent<br>14. A multicarrier system including a first transceiver that uses a plurality of carrier signals for modulating a bit stream, wherein **each carrier signal has a phase characteristic associated with the bit stream**, the transceiver capable of: associating each carrier signal with a value determined independently of any bit value of the bit stream carried by that respective carrier signal, the value associated with each carrier signal determined using a pseudo-random number generator; computing a phase shift for each carrier signal based on the value associated with that carrier signal; and combining the phase shift computed for each respective carrier signal with the **phase characteristic** of that carrier signal to substantially scramble the **phase characteristics** of the plurality of carrier signals, wherein multiple carrier | 11 | "one or more values that represent the angular aspect of a carrier signal" | Plain and ordinary meaning | |

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| signals corresponding to the scrambled carrier signals are used by the first transceiver to modulate the same bit value. | | | | |
| "substantially scramble the phase characteristics of the plurality of carrier signals"<br><br>Family 4<br>'008 Patent, claim 14<br><br>'008 Patent<br>14. A multicarrier system including a first transceiver that uses a plurality of carrier signals for modulating a bit stream, wherein each carrier signal has a phase characteristic associated with the bit stream, the transceiver capable of: associating each carrier signal with a value determined independently of any bit value of the bit stream carried by that respective carrier signal, the value associated with each carrier signal determined using a pseudo-random number generator; computing a phase shift for each carrier signal based on the value associated with that carrier signal; and combining the phase shift computed for each respective carrier signal with the phase characteristic of that carrier signal | 12 | "adjust the phase characteristics of the carrier signals by varying amounts to produce a transmission signal with a reduced peak to-average power ratio (PAR)" | Plain and ordinary meaning | |

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| to **substantially scramble the phase characteristics of the plurality of carrier signals**, wherein multiple carrier signals corresponding to the scrambled carrier signals are used by the first transceiver to modulate the same bit value. | | | | |
| "same bit value"<br><br>Family 4<br>'008 Patent, claim 14<br><br>'008 Patent<br>14. A multicarrier system including a first transceiver that uses a plurality of carrier signals for modulating a bit stream, wherein each carrier signal has a phase characteristic associated with the bit stream, the transceiver capable of: associating each carrier signal with a value determined independently of any bit value of the bit stream carried by that respective carrier signal, the value associated with each carrier signal determined using a pseudo-random number generator; computing a phase shift for each carrier signal based on the value associated with that carrier signal; and combining the phase shift computed for each respective carrier signal with the | 13 | "value of the same bit" | Indefinite. | |

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| phase characteristic of that carrier signal to substantially scramble the phase characteristics of the plurality of carrier signals, wherein multiple carrier signals corresponding to the scrambled carrier signals are used by the first transceiver to modulate the **same bit value**. | | | | |
| "multiple carrier signals corresponding to the scrambled carrier signals are used by the first multicarrier transceiver to modulate the same bit value"<br><br>Family 4<br>'008 Patent, claim 14<br><br>'008 Patent<br>14. A multicarrier system including a first transceiver that uses a plurality of carrier signals for modulating a bit stream, wherein each carrier signal has a phase characteristic associated with the bit stream, the transceiver capable of: associating each carrier signal with a value determined independently of any bit value of the bit stream carried by that respective carrier signal, the value associated with each carrier signal determined using a pseudo-random number generator; computing a phase shift for each carrier signal based on the | 14 | "a first carrier signal is used by the first multicarrier transceiver to demodulate the value of a bit of the received bit stream and at least one more carrier signal is used by the first multi carrier transceiver to demodulate the value of the same bit of the received bit stream, wherein the carrier signals correspond to the plurality of phase-shifted and scrambled carrier signals." | Indefinite. | |

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| value associated with that carrier signal; and combining the phase shift computed for each respective carrier signal with the phase characteristic of that carrier signal to substantially scramble the phase characteristics of the plurality of carrier signals, wherein **multiple carrier signals corresponding to the scrambled carrier signals are used by the first transceiver to modulate the same bit value**. | | | | |
| "computing a phase shift for each carrier signal"<br><br>Family 4<br>'008 Patent, claim 14<br><br>'008 Patent<br>14. A multicarrier system including a first transceiver that uses a plurality of carrier signals for modulating a bit stream, wherein each carrier signal has a phase characteristic associated with the bit stream, the transceiver capable of: associating each carrier signal with a value determined independently of any bit value of the bit stream carried by that respective carrier signal, the value associated with each carrier signal determined using a pseudo-random | 15 | Plain and ordinary meaning. No construction necessary. | "computing the amount by which a phase is adjusted for each carrier signal" | |

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| number generator; **computing a phase shift for each carrier signal** based on the value associated with that carrier signal; and combining the phase shift computed for each respective carrier signal with the phase characteristic of that carrier signal to substantially scramble the phase characteristics of the plurality of carrier signals, wherein multiple carrier signals corresponding to the scrambled carrier signals are used by the first transceiver to modulate the same bit value. | | | | |
| "combining the phase shift computed for each respective carrier signal with the phase characteristic of that carrier signal"<br><br><u>Family 4</u><br>'008 Patent, claim 14<br><br><u>'008 Patent</u><br>14. A multicarrier system including a first transceiver that uses a plurality of carrier signals for modulating a bit stream, wherein each carrier signal has a phase characteristic associated with the bit stream, the transceiver capable of: associating each carrier signal with a value determined independently of any bit value of the bit stream carried by that | 16 | Plain and ordinary meaning. No construction necessary. | "adjusting the phase of each carrier signal by an amount computed for that carrier signal" | |

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| respective carrier signal, the value associated with each carrier signal determined using a pseudo-random number generator; computing a phase shift for each carrier signal based on the value associated with that carrier signal; and **combining the phase shift computed for each respective carrier signal with the phase characteristic of that carrier signal** to substantially scramble the phase characteristics of the plurality of carrier signals, wherein multiple carrier signals corresponding to the scrambled carrier signals are used by the first transceiver to modulate the same bit value. | | | | |
| "steady-state communication"<br><br><u>Family 6</u><br>'835 Patent, claim 8<br>'112 Patent, claim 8<br><br><u>'835 Patent</u><br>8. An apparatus configurable to adapt forward error correction and interleaver parameter (FIP) settings during **steady-state communication** or initialization comprising: a transceiver, including a processor, configurable to: transmit a signal using a first FIP setting, transmit a | 17 | "Showtime" | "the state of the transceiver reached after all initialization and training is completed in which user data is transmitted or received" | |

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| flag signal, and switch to using for transmission, a second FIP setting following transmission of the flag signal, wherein: the first FIP setting comprises at least one first FIP value, the second FIP setting comprises at least one second FIP value, different than the first FIP value, and the switching occurs on a pre-defined forward error correction codeword boundary following the flag signal.<br><br>'112 Patent<br>8. A transceiver comprising: a receiver operable to receiving, during **steady-state communication**, using a first forward error correction and interleaving parameter (FIP) setting that comprises a forward error correction (FEC) codeword size and a first number of FEC coding parity bytes; and the receiver further operable to switch, during the **steady-state communication**, to receiving using a second FIP setting that comprises a second FEC codeword size that is different than the first FEC codeword size and a second number of FEC coding parity bytes that is different than the first number of FEC coding parity bytes, | | | | |

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| wherein the switching to receiving using the second FEC codeword size and the second number of FEC coding parity bytes is based on a counter reaching a value. | | | | |
| "FIP setting"<br><br><u>Family 6</u><br>'835 Patent, claims 8, 10, and 26<br>'112 Patent, claim 8<br><br><u>'835 Patent</u><br>8. An apparatus configurable to adapt forward error correction and interleaver parameter **(FIP) settings** during steady-state communication or initialization comprising: a transceiver, including a processor, configurable to: transmit a signal using a first **FIP setting**, transmit a flag signal, and switch to using for transmission, a second **FIP setting** following transmission of the flag signal, wherein: the first **FIP setting** comprises at least one first FIP value, the second **FIP setting** comprises at least one second FIP value, different than the first FIP value, and the switching occurs on a pre-defined forward error correction | 18 | Plain and ordinary meaning. No construction necessary. | "forward error correction and interleaver parameters characterized by the set of parameters for codeword size in bytes, number of information bytes in a codeword, number of parity or redundancy bytes in a codeword, and interleaver depth in number of codewords" | |

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| codeword boundary following the flag signal.<br><br>10. The apparatus of claim 8, wherein a first interleaver parameter value of the first **FIP setting** is different than a second interleaver parameter value of the second **FIP setting**.<br><br>26. The apparatus of claim 24, wherein a first interleaver parameter value of the first **FIP setting** is different than a second interleaver parameter value of the second **FIP setting**.<br><br><br><u>'112 Patent</u><br>8. A transceiver comprising: a receiver operable to receiving, during steady-state communication, using a first forward error correction and interleaving parameter **(FIP) setting** that comprises a forward error correction (FEC) codeword size and a first number of FEC coding parity bytes; and the receiver further operable to switch, during the steady-state communication, to receiving using a second **FIP setting** that comprises a second FEC codeword size that is different than the first FEC codeword | | | | |

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| size and a second number of FEC coding parity bytes that is different than the first number of FEC coding parity bytes, wherein the switching to receiving using the second FEC codeword size and the second number of FEC coding parity bytes is based on a counter reaching a value. | | | | |
| "FIP value"<br><br><u>Family 6</u><br>'835 Patent, claim 8<br><br><u>'835 Patent</u><br>8. An apparatus configurable to adapt forward error correction and interleaver parameter (FIP) settings during steady-state communication or initialization comprising: a transceiver, including a processor, configurable to: transmit a signal using a first FIP setting, transmit a flag signal, and switch to using for transmission, a second FIP setting following transmission of the flag signal, wherein: the first FIP setting comprises at least one first **FIP value**, the second FIP setting comprises at least one second **FIP value**, different than the first **FIP value**, and the switching occurs on a pre-defined forward error correction | 19 | Plain and ordinary meaning. No construction necessary. | "numerical value of codeword size in bytes, number of information bytes in a codeword, number of parity or redundancy bytes in a codeword, or interleaver depth in number of codewords" | |

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| codeword boundary following the flag signal. | | | | |
| "flag signal"<br><br><u>Family 6</u><br>'835 Patent, claim 8<br>'162 Patent, claims 8 and 9<br><br><u>'835 Patent</u><br>8. An apparatus configurable to adapt forward error correction and interleaver parameter (FIP) settings during steady-state communication or initialization comprising: a transceiver, including a processor, configurable to: transmit a signal using a first FIP setting, transmit a **flag signal**, and switch to using for transmission, a second FIP setting following transmission of the **flag signal**, wherein: the first FIP setting comprises at least one first FIP value, the second FIP setting comprises at least one second FIP value, different than the first FIP value, and the switching occurs on a pre-defined forward error correction codeword boundary following the **flag signal**.<br><br><u>'162 Patent</u> | 20 | "signal used to indicate when an updated FIP setting / interleaver parameter value is to be used (the signal does not contain message data indicating when the updated FIP setting/ interleaver parameter value is to be used)" | "signal used to indicate when updated FIP settings / interleaver parameter values are to be used" | |

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| 8. A device comprising: an interleaver configured to interleave a plurality of bits; and a transmitter portion coupled to the interleaver and configured to: transmit using a first interleaver parameter value; transmit a **flag signal**; and change to transmitting using a second interleaver parameter value that is different than the first interleaver parameter value, wherein the second interleaver parameter value is used for transmission on a pre-defined forward error correction codeword boundary following transmission of the **flag signal**.<br><br>9. The device of claim 8, wherein the **flag signal** is an inverted sync symbol. | | | | |
| "interleaver parameter value"<br><br><u>Family 6</u><br>'835 Patent, claims 10 and 26<br>'162 Patent, claim 8<br><br><u>'835 Patent</u><br>10. The apparatus of claim 8, wherein a first **interleaver parameter value** of the first FIP setting is different than a second **interleaver parameter value** of the second FIP setting. | 21 | Plain and ordinary meaning. No construction necessary. | "the numerical value of the interleaver depth in number of codewords" | |

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| 26. The apparatus of claim 24, wherein a first **interleaver parameter value** of the first FIP setting is different than a second **interleaver parameter value** of the second FIP setting.<br><br>'162 Patent<br>8. A device comprising: an interleaver configured to interleave a plurality of bits; and a transmitter portion coupled to the interleaver and configured to: transmit using a first **interleaver parameter value**; transmit a flag signal; and change to transmitting using a second **interleaver parameter value** that is different than the first **interleaver parameter value**, wherein the second **interleaver parameter value** is used for transmission on a pre-defined forward error correction codeword boundary following transmission of the flag signal. | | | | |
| "higher immunity to noise"<br><br>Family 9<br>'348 Patent, claim 2<br><br>'348 Patent<br>2. The apparatus of claim 1, wherein the received messages have a **higher** | 22 | "higher SNR margin" | plain and ordinary meaning | |

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| **immunity to noise** than the transmitted packet. | | | | |
| "receive at least one packet using deinterleaving, and transmit at least one message without using interleaving"<br><br>Family 9<br>'577 Patent, claim 16<br><br>16. An apparatus comprising: a multicarrier transceiver operable to **receive at least one packet using deinterleaving, and transmit at least one message without using interleaving**, wherein the at least one message includes information that indicates an acknowledgement (ACK) or a negative acknowledgement (NACK) of the at least one packet, wherein the at least one packet comprises one or more PTM-TC codewords. | 23 | Plain and ordinary meaning. No construction necessary. | Indefinite. | |
| "[transmit/receive] a [packet/plurality of messages] using a forward error correction [encoder/decoder] and [without using] [an/a interleaver/deinterleaver]"<br><br>Family 9 | 24 | Plain and ordinary meaning. No construction necessary. | Indefinite. | |

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| '348 Patent, claims 1 and 9<br><br>'348 Patent<br><br>1. An apparatus comprising: a multicarrier transceiver including a processor and memory operable to: **transmit a packet using a forward error correction encoder and an interleaver**, wherein the packet comprises a header field and a plurality of PTM-TC codewords, a plurality of ATM cells or a plurality of Reed-Solomon codewords, and wherein the header field comprises a sequence identifier (SID); and **receive a plurality of messages using a forward error correction decoder and without using a deinterleaver**, wherein each message of the plurality of messages is received in a different DMT symbol and wherein at least one message of the plurality of messages includes an acknowledgement (ACK) or a negative acknowledgement (NACK) of the transmitted packet.<br><br>9. An apparatus comprising: a multicarrier transceiver including a processor and memory operable to: **receive a packet using a forward error** | | | | |

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| **correction decoder and a deinterleaver**, wherein the packet comprises a header field and a plurality of PTM-TC codewords, a plurality of ATM cells or a plurality of Reed-Solomon codewords, and wherein the header field comprises a sequence identifier (SID); and **transmit a plurality of messages using a forward error correction encoder and without using an interleaver**, wherein each message of the plurality of messages is transmitted in a different DMT symbol and wherein at least one message of the plurality of messages includes an acknowledgement (ACK) or a negative acknowledgement (NACK) of the received packet. | | | | |
| "[transmitting/receiving] a [packet/message] using forward error correction [encoding/decoding] and [without using] [interleaving/deinterleaving]"<br><br>Family 9<br>'809 Patent, claim 8<br><br>'809 Patent | 25 | Plain and ordinary meaning. No construction necessary. | Indefinite. | |

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| 8. An apparatus comprising: a multicarrier transceiver including a processor and memory capable of: **receiving a packet using forward error correction decoding and deinterleaving**, wherein the packet comprises a header field and a plurality of Reed-Solomon codewords, and wherein the header field comprises a sequence identifier (SID); and **transmitting a message using forward error correction encoding and without using interleaving**, wherein the message is transmitted in a single DMT symbol and wherein the message includes an acknowledgement (ACK) or a negative acknowledgement (NACK) of the received packet. | | | | |
| "A multicarrier communications transceiver operable to: receive a multicarrier symbol comprising a first plurality of carriers"<br><br>Family 10<br>'354 Patent, claim 10<br><br>'354 Patent<br>10. **A multicarrier communications transceiver operable to: receive a multicarrier symbol comprising a first** | 26 | Plain and ordinary meaning. No construction necessary. | Indefinite. | |

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| **plurality of carriers** and a second plurality of carriers; receive a first plurality of bits on the first plurality of carriers using a first SNR margin; receive a second plurality of bits on the second plurality of carriers using a second SNR margin; wherein the first plurality of carriers is different than the second plurality of carriers, wherein the first SNR margin is different than the second SNR margin, and wherein the first SNR margin provides more robust reception. | | | | |
| "receive a first plurality of bits on the first plurality of carriers using a first SNR margin;<br>receive a second plurality of bits on the second plurality of carriers using a second SNR margin"<br><br><u>Family 10</u><br>'354 Patent, claim 10<br><br><u>'354 Patent</u><br>10. A multicarrier communications transceiver operable to: receive a multicarrier symbol comprising a first plurality of carriers and a second plurality of carriers; **receive a first plurality of bits on the first plurality of carriers using a first SNR margin;** | 27 | Plain and ordinary meaning. No construction necessary. | Indefinite. | |

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| **receive a second plurality of bits on the second plurality of carriers using a second SNR margin**; wherein the first plurality of carriers is different than the second plurality of carriers, wherein the first SNR margin is different than the second SNR margin, and wherein the first SNR margin provides more robust reception. | | | | |
| "wherein the first SNR margin provides more robust reception than the second SNR margin"<br><br><u>Family 10</u><br>'354 Patent, claim 10<br><br><u>'354 Patent</u><br>10. A multicarrier communications transceiver operable to: receive a multicarrier symbol comprising a first plurality of carriers and a second plurality of carriers; receive a first plurality of bits on the first plurality of carriers using a first SNR margin; receive a second plurality of bits on the second plurality of carriers using a second SNR margin; wherein the first plurality of carriers is different than the second plurality of carriers, wherein the first SNR margin is different than the second | 28 | Plain and ordinary meaning. No construction necessary. | Indefinite. | |

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| SNR margin, and **wherein the first SNR margin provides more robust reception**. | | | | |
| "signal to noise ratio (SNR) margin" / "SNR margin"<br><br><u>Family 10</u><br>'988 Patent, claim 16<br>'354 Patent, claims 10<br><br><u>'988 Patent</u><br><br>16. An apparatus comprising: a multicarrier communications transceiver operable to demodulate for reception a first plurality of bits from a first carrier using a first **Signal to Noise Ratio (SNR) margin** and to demodulate for reception a second plurality of bits from a second carrier using a second **SNR margin**, and to demodulate for reception a third plurality of bits from the first carrier using a third **SNR margin**, wherein the first **SNR margin** specifies a first value for an allowable increase in noise without an increase in the bit error rate (BER) associated with the first carrier, wherein the second **SNR margin** specifies a second value for an allowable increase in noise without an increase in | 29 | Plain and ordinary meaning. No construction necessary. | a parameter used in determining the number of bits allocated to each of a plurality of carriers, where the value of the parameter specifies an extra SNR requirement assigned per carrier in addition to the SNR required to maintain a specified bit error rate (BER) for the communication link at a specified bit allocation | |

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| the bit error rate (BER) associated with the second carrier, wherein the third **SNR margin** specifies a third value for an allowable increase in noise without an increase in the bit error rate (BER) associated with said first carrier, wherein the first **SNR margin** is different than the second **SNR margin**, wherein the first **SNR margin** is different than the third **SNR margin**, and wherein the first plurality of bits, the second plurality of bits and the third plurality of bits are each different from one another.<br><br>'354 Patent<br>10. A multicarrier communications transceiver operable to: receive a multicarrier symbol comprising a first plurality of carriers and a second plurality of carriers; receive a first plurality of bits on the first plurality of carriers using a first **SNR margin**; receive a second plurality of bits on the second plurality of carriers using a second **SNR margin**; wherein the first plurality of carriers is different than the second plurality of carriers, wherein the first **SNR margin** is different than the second **SNR margin**, and wherein the | | | | |

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| first **SNR margin** provides more robust reception. | | | | |